

Amendments to the Claims

1. (Currently Amended) A circuit arrangement ~~(100)~~ for protecting a chip arrangement (200), comprising:

at least one optosensitive detector unit ~~(10)~~, comprising at least one bipolar transistor, whose output voltage ( $V_{out}$ ) is a measure of the incidence of light ( $L_i$ ) on the detector unit ~~(10)~~, and

at least one comparator unit (20) preceded by the detector unit ~~(10)~~ provided for comparing the output voltage ( $V_{out}$ ) of the detector unit ~~(10)~~ with a reference voltage ( $V_{ref}$ ), wherein the data and/or functions of the chip arrangement (200) to be protected can be temporarily or permanently obstructed, and/or erased, ( $L_i$ ) and/or blocked, ( $S$ ) and/or interrupted in the case of a failure message occurring during comparison of the output voltage ( $V_{out}$ ) of the detector unit ~~(10)~~ with the reference voltage ( $V_{ref}$ ).

2. (Currently Amended) A circuit arrangement ~~(100)~~ as claimed in claim 1, characterized in that wherein the detector unit ~~(10)~~ is arranged

underneath at least an oxide layer of the chip arrangement (200), and/or substantially in the plane of the data and/or functions to be protected.

3. (Previously Cancelled).

4. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, ~~characterized in that~~ wherein the detector unit (10) ~~is constituted by~~ comprises a plurality of spatially arranged bipolar transistors (12).

5. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, ~~characterized in that~~ wherein an emitter (124) of the bipolar transistor (12) is connected to ~~the~~ an input (22), provided for the output voltage ( $V_{out}$ ), of the comparator unit (20).

6. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, ~~characterized in that~~ wherein an emitter (124) of the bipolar transistor (12) is connected to at least a power supply voltage ( $V_{dd}$ ) via at least a power supply resistor (14).

7. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, ~~characterized in that~~ wherein a collector (126) of the bipolar transistor (12) is connected to ground potential via at least a reference resistor (16).

8. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, ~~characterized in that~~ wherein a junction between a base (122) of the bipolar transistor (12) and a collector (126) of the bipolar transistor (12) is provided for absorbing the light incident on the detector unit (10).

9. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that wherein the output voltage ( $V_{out}$ ) of the detector unit (10) depends on a wavelength and/or an intensity of the incident light ( $L_i$ ).

10. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that wherein

at least an evaluation unit (30) is implemented and/or integrated in the comparator unit (20), or

the comparator unit (20) precedes at least an evaluation unit (30).

11. (Currently Amended) A circuit arrangement (100) as claimed in claim 10, characterized in that wherein the evaluation unit (30) generates the failure message when the output voltage ( $V_{out}$ ) of the detector unit (10) deviates from a nominal range.

12. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that wherein

a working point of the detector unit (10) and/or

a threshold value of the reference voltage ( $V_{ref}$ ) is adjustable.

13. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that further comprising at least a dielectric coating and/or a further protective coating which is

provided for protecting the chip arrangement (200) from external influences is arranged within the chip arrangement (200) and/or laterally to the chip arrangement (200) and/or on the chip arrangement (200).

14. (Currently Amended) A circuit arrangement (100) as claimed in claim 13, characterized in that wherein a material of the ~~dielectric~~ protective coating is selected from the group consisting of epoxy resin, or silicon nitrite (SiNO<sub>2</sub>), or and silicon dioxide (SiO<sub>2</sub>).

15. (Currently Amended) A circuit arrangement (100) as claimed in claim 13, characterized in that wherein a material of the ~~dielectric~~ protective coating is substantially opaque.

16. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that wherein the chip arrangement (200) is arranged on at least a layered carrier substrate of a semiconducting or insulating material.

17. (Currently Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that wherein the circuit arrangement (100) is implemented and/or integrated in a card.

18. (Currently Amended) A card, comprising the circuit arrangement (100) as claimed in claim 1.

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19. (Currently Amended) A chip arrangement (200), comprising
- at least one optosensitive detector units (40) as claimed in claim 1, and
  - at least a combination logic unit (40) for combining the detector units (40).
20. (Currently Amended) A chip arrangement (200) as claimed in claim 19, ~~characterized in that~~ wherein the combination logic unit (40) is connected to at least a control logic unit (50).
21. (Currently Amended) A chip arrangement (200) as claimed in claim 19, ~~characterized in that~~ wherein the combination logic unit (40) is connected to an electrically erasable storage unit (60).
22. (Currently Amended) A chip arrangement (200) as claimed in claim 21, ~~characterized in that~~ wherein the storage unit (60) is constituted by at least an Electrically Erasable Programmable Read-Only Memory (EEPROM) storage unit (60) ~~(EEPROM = Electrically Erasable Programmable Read-Only Memory)~~, and the data and/or functions of the chip arrangement (200) to be protected are erasable (~~±~~) when a failure message by means of the EEPROM storage unit (60) occurs during comparison of the output voltage ( $V_{out}$ ) of the detector unit (40) with the reference voltage ( $V_{ref}$ ).
23. (Currently Amended) A chip arrangement (200) as claimed in claim 20, ~~characterized in that~~ wherein

the storage unit ~~(60)~~ is arranged between the combination logic unit ~~(40)~~ and the control logic unit ~~(50)~~, and

~~the~~ access to the data and/or functions of the chip arrangement ~~(200)~~ to be protected can be blocked by blocking ~~(S)~~ the storage unit ~~(60)~~ when a failure message occurs during comparison of the output voltage ( $V_{out}$ ) of the detector unit ~~(10)~~ with the reference voltage ( $V_{ref}$ ).

24. (Currently Amended) A chip arrangement ~~(200)~~ as claimed in claim 19, ~~characterized in that~~ wherein the chip arrangement ~~(200)~~ can be permanently short-circuited via the power supply voltage ( $V_{dd}$ ).

25. (Currently Amended) A method of protecting a chip arrangement ~~(200)~~, ~~characterized in that~~ wherein

an output voltage ( $V_{out}$ ) determined by light ~~(L)~~ incident on a detector unit ~~(10)~~ is generated in an optosensitive detector unit ~~(10)~~ comprising a bipolar transistor;

the output voltage ( $V_{out}$ ) of the detector unit ~~(10)~~ is compared with a reference voltage ( $V_{ref}$ ) in a comparator unit ~~(20)~~ preceded by the detector unit ~~(10)~~, and

the data and/or functions of the chip arrangement ~~(200)~~ to be protected are ~~temporarily or permanently obstructed, and/or erased, (L) and/or blocked, (S) and/or interrupted~~ when a failure message is generated during comparison of the output voltage ( $V_{out}$ ) of the detector unit ~~(10)~~ with the reference voltage ( $V_{ref}$ ).

26. (Currently Amended) A method as claimed in claim 25, ~~characterized in that~~ wherein the light incident on the detector unit (10) is substantially absorbed by means of a junction between a base (122) of the bipolar transistor (12) and a collector (126) of the bipolar transistor (12).

27. (Currently Amended) A method as claimed in claim 25, ~~characterized in that~~ wherein the failure message is triggered in the comparator unit (20) when the output voltage ( $V_{out}$ ) of the detector unit (10) deviates from a nominal range.

28. (Currently Amended) A method as claimed in claim 25, ~~characterized in that~~ wherein the triggering of the failure message is adjusted by means of

a working point of the detector unit (10) and/or

a threshold value of the reference voltage ( $V_{ref}$ ).

29. (Currently Amended) A method as claimed in claim 25, ~~characterized in that~~ wherein the failure message is generated in at least

an evaluation unit (30) implemented and/or integrated in the comparator unit (20),

or

an evaluation unit (30) preceded by the comparator unit (20).

30. (Currently Amended) A method as claimed in claim 25, ~~characterized in that~~ wherein a control logic unit (50) connected to a combination logic unit (40) provided for combining the detector units (10) is temporarily blocked (S) when the failure message is triggered.

31. (Currently Amended) A method as claimed in claim 25, ~~characterized in that~~ wherein an electrically erasable storage unit (60) arranged between at least a combination logic unit (40) provided for combining the detector units (10) and a control logic unit (50) is permanently blocked (S) when the failure message is triggered.

32. (Currently Amended) A method as claimed in claim 31, ~~characterized in that~~ wherein the control logic unit (50) is temporarily or permanently blocked (S) by means of at least a "reset" (RS).

33. (Currently Amended) A method as claimed in claim 25, ~~characterized in that~~ wherein a once-electrically programmable storage unit (60) connected to a combination logic unit (40) provided for combining the detector units (10) is permanently blocked (S) when the failure message is triggered.

34. (Currently Amended) A method as claimed in claim 33, ~~characterized in that~~ wherein the power supply voltage ( $V_{dd}$ ) is short-circuited by means of the storage unit (60).



35. (Currently Amended) A method as claimed in claim 25, ~~characterized in that~~ wherein the data and/or functions to be protected are erased ~~(L)~~ in an Electrically Erasable Programmable Read-Only Memory (EEPROM) storage unit ~~(60)~~ ~~(EEPROM = Electrically Erasable Programmable Read-Only Memory)~~ connected to a combination logic unit ~~(40)~~ provided for combining the detector units ~~(40)~~ when the failure message is triggered.